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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KROFCHECK, MICHAEL C	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 10/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,840	DAY ET AL.	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/20/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/670,840 filed on September 25, 2003.

2. Claims 1 – 27 have been submitted for examination.

3. Claims 1 – 27 have been examined.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: figure 50, reference number 5010 which is mentioned in the last paragraph on page 57 of the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The abstract of the disclosure is objected to because:

a. In the title at the top of the abstract, the word "system" is missing the letter "e"

b. In line 8 of the abstract, the word "are" should be replaced by "is"

c. In line 10 of the abstract, the word "is" should be replaced by "are"

Correction is required. See MPEP § 608.01(b).

6. The disclosure is objected to because of the following informalities:

a. In line 7 of page 3, the word "are" should be replaced by "is"

b. The word, "A" should be included on page 18 as the first word on line 25.

c. The last paragraph of page 57 incorrectly describes figure 50. Reference number 5010 is described as both an SPU and a PU (reference number 5010 appears to have been mistakenly omitted from figure 50). SPU 5020 is described as accessing block 5055, while it actually accesses block 5050, which is described as being accessed by SPU 5010 (not shown).

d. The brief description of figure 2 states that it is the structure of a processing unit (PU), however the respective figure indicates it is a processor element (PE).

e. The specification appears to interchangeably use the terms "processing element" or "PE" and "processing unit" or "PU" throughout the specification. For example: pages 12 – 14 discuss figure 2. Looking at figure 2, one sees a processor element, 201. However, the specification refers to 201 as a

processing unit, PU. The specification also refers to 203 as a PU, which is a subset of 201. It is clear from the specification that 201 and 203 are not intended to be the same thing. 203 is a processor capable of stand-alone processing, while 201 appears to be a grouping of a PU (203), SPU and other modules that work under control of the PU (203) to process data and applications. The examiner has noticed numerous other instances throughout the specification and drawings where the processor element is mistakenly referred to as a processing unit. This makes it quite difficult to understand the applicant's intentions. The examiner respectfully requests that the applicant double check and correct the specification and drawings to ensure that where the applicant intends to discuss the processor element, the applicant uses the term "processor element" or "PE," and not "processor unit" or "PU."

Appropriate correction is required.

7. The lengthy specification has not been checked to the extent necessary to determine the presence of *all possible* minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1 – 6, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuoki at al U.S. Patent No. 6,526,491 (hereinafter Suzuoki) and an admission of prior art by the applicant.

11. With respect to claim 1, Suzuoki teaches of a computer-implemented method for handling data using a plurality of processors, the method comprising: dividing a common memory, accessible to one or more first processors and to one or more secondary processors, into a plurality of data blocks using one of the first processors (figs. 2, 24; item 2412; column 3, lines 43 – 53; column 7, lines 43 – 56; column 18, lines 32 – 35; where the processing unit allocates space in the DRAM for executing the apulet by issuing a DMA command to the DMAC to setup the necessary sandboxes. The sandboxes are exclusive areas in the DRAM which only a specific attached processing unit can access),

identifying an available processor from the secondary processors to process one of the data blocks (fig. 24; item 2410; column 7, lines 57 – 66; column 18, lines 31 – 32;

where the processing unit designates an attached processing unit to process the apulet);

and processing the data block using the available secondary processor (fig. 24; item 2438; column 7, lines 57 – 66; column 18, lines 66 – 67; where the attached processing unit processes the apulet and generates a result).

Suzuoki fails to specifically teach of the one or more first processors and the one or more second processors being chosen from a group of heterogeneous processors. However, the applicant admits as prior art that the one or more first processors and the one or more second processors being chosen from a group of heterogeneous processors (applicant's specification page 1, lines 12 – 19; where the multiple processors are dissimilar, with each processor specializing in a particular processing task).

Suzuoki and the applicant's admission are analogous arts as they are both in the same field of endeavor, sharing a common memory in a multiprocessor system. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the multiple processors (PUs and APUs) in Suzuoki be different as is admitted prior art by the applicant. Suzuoki expresses the desire for the network to include a multitude of different computing devices, such as PCs, PDAs, appliances, and others (column 2, lines 61 – 64). To accomplish this, having multiple processors that are dissimilar, that is each processor specializing in a specific task, is necessary.

12. With respect to claim 2, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki also teaches of

directly accessing the data block in the common memory using a memory access unit of the available secondary processor (fig. 17E; item 1742; column 13, lines 9 – 18; where the control logic issues a command which reads a memory location in the DRAM).

13. With respect to claim 3, the combination of Suzuoki and the admission teach of all the limitations of the parent claims as discussed supra. Suzuoki also teaches of transferring the data block using the available secondary processor from the common memory to a secondary memory local to the available secondary processor (figs. 17G, 24; items 2434, 2436; column 13, lines 19 – 21; column 18, lines 61 – 66; where the data is read from the DRAM into the local storage of the attached processing unit).

14. With respect to claim 4, the combination of Suzuoki and the admission teach of all the limitations of the parent claims as discussed supra. Suzuoki also teaches of transferring the data block using the available secondary processor from the secondary memory to the common memory after processing the data block (fig. 24; items 2440, 2442; column 18, line 67 – column 19, line 4; where the APU issues a DMA command to store the result in the DRAM from the APU's local memory).

15. With respect to claim 5, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki also teaches of the available secondary processor notifying one of the first processors after processing the data block (fig. 24; item 2444; column 19, line 4 – 6; where the APU issues an interrupt request to the PU to signal that the processing is complete).

16. With respect to claim 6, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki also teaches of

requesting, using one of the first processors, the secondary processor to process the data block (fig. 24; item 2410; column 18, lines 31 – 32; where the processing unit designates an APU to process the apulet).

17. With respect to claim 8, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki also teaches of processing the data block further using one of the first processors (fig. 24; item 2410; column 18, lines 31 – 32; where the processing unit evaluates the apulet before designating an APU to process it).

18. With respect to claim 10 Suzuoki teaches of an information handling system comprising a plurality of processors (figs. 2, 3; column 7, lines 19 – 25),

wherein the plurality of processors comprises one or more first processors and one or more secondary processors (figs. 2, 3; column 7, lines 19 – 25; column 8, lines 9 – 10; where the processors comprise processing units, PUs (first processors) and attached processing units, APUs (secondary processors));

and a common memory accessible by the plurality of processors (figs. 2, 3; items 225, 315; column 7, lines 42 – 52; where the DRAM is accessed by the processors, PU and APU alike),

wherein one of the first processors is adapted to divide the common memory into a plurality of data blocks (figs. 2, 24; item 2412; column 3, lines 43 – 53; column 7, lines 43 – 56; column 18, lines 32 – 35; where the processing unit allocates space in the DRAM for executing the apulet by issuing a DMA command to the DMAC to setup the

necessary sandboxes. The sandboxes are exclusive areas in the DRAM which only a specific attached processing unit can access),

one of the first processors is adapted to identify an available processor from the secondary processors to process one of the data block (fig. 24; item 2410; column 7, lines 57 – 66; column 18, lines 31 – 32; where the processing unit designates an attached processing unit to process the apulet);

and one of the secondary processors is adapted to process the data block (fig. 24; item 2438; column 7, lines 57 – 66; column 18, lines 66 – 67; where the attached processing unit processes the apulet and generates a result).

Suzuoki fails to specifically teach of a plurality of heterogeneous processors. However, the applicant's admitted prior art teaches of a plurality of heterogeneous processors (applicant's specification page 1, lines 12 – 19; where the multiple processors are dissimilar, with each processor specializing in a particular processing task).

19. With respect to claim 11, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki also teaches of wherein the available secondary processor is further adapted to directly access the data block in the common memory using a memory access unit (fig. 17E; item 1742; column 13, lines 9 – 18; where the control logic issues a command which reads a memory location in the DRAM).

20. With respect to claim 12, the combination of Suzuoki and the admission teach of all the limitations of the parent claims as discussed supra. Suzuoki also teaches of

wherein the available secondary processor is further adapted to transfer the data block from the common memory to a secondary memory local to the available secondary processor (figs. 17G, 24; items 2434, 2436; column 13, lines 19 – 21; column 18, lines 61 – 66; where the data is read from the DRAM into the local storage of the attached processing unit).

21. With respect to claim 13, the combination of Suzuoki and the admission teach of all the limitations of the parent claims as discussed supra. Suzuoki also teaches of wherein the available secondary processor is further adapted to transfer the data block from the secondary memory to the common memory after processing the data block (fig. 24; items 2440, 2442; column 18, line 67 – column 19, line 4; where the APU issues a DMA command to store the result in the DRAM from the APU's local memory).

22. With respect to claim 14, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki also teaches of wherein the available secondary processor is further adapted to notify one of the first processors after processing the data block (fig. 24; item 2444; column 19, line 4 – 6; where the APU issues an interrupt request to the PU to signal that the processing is complete).

23. With respect to claim 15, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki also teaches of wherein one of the first processors is adapted to request the available secondary processor to process the data block (fig. 24; item 2410; column 18, lines 31 – 32; where the processing unit designates an APU to process the apulet).

24. With respect to claim 17, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki also teaches of wherein one of the first processors is adapted to further process the data block (fig. 24; item 2410; column 18, lines 31 – 32; where the processing unit evaluates the apulet before designating an APU to process it).

25. With respect to claim 19, Suzuoki teaches of a computer program product on computer operable media, the computer program product comprising: means for dividing a common memory, accessible to one or more first processors and to one or more secondary processors, into a plurality of data blocks (figs. 2, 24; item 2412; column 3, lines 43 – 53; column 7, lines 43 – 56; column 18, lines 32 – 35; where the processing unit allocates space in the DRAM for executing the apulet by issuing a DMA command to the DMAC to setup the necessary sandboxes. The sandboxes are exclusive areas in the DRAM which only a specific attached processing unit can access),

means for identifying an available processor from the secondary processors to process one of the data blocks (fig. 24; item 2410; column 7, lines 57 – 66; column 18, lines 31 – 32; where the processing unit designates an attached processing unit to process the apulet); and

means for processing the data block using the available secondary processor (fig. 24; item 2438; column 7, lines 57 – 66; column 18, lines 66 – 67; where the attached processing unit processes the apulet and generates a result).

Suzuoki fails to specifically teach of wherein the one or more first processors and the one or more second processors are selected from a group of heterogeneous processors. However, the applicant's admitted prior art teaches of wherein the one or more first processors and the one or more second processors are selected from a group of heterogeneous processors (applicant's specification page 1, lines 12 – 19; where the multiple processors are dissimilar, with each processor specializing in a particular processing task).

26. With respect to claim 20, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki also teaches of means for directly accessing the data block in the common memory (fig. 17E; item 1742; column 13, lines 9 – 18; where the control logic issues a command which reads a memory location in the DRAM).

27. With respect to claim 21, the combination of Suzuoki and the admission teach of all the limitations of the parent claims as discussed supra. Suzuoki also teaches of means for transferring the data block from the common memory to a secondary memory local to the available secondary processor (figs. 17G, 24; items 2434, 2436; column 13, lines 9 – 21; column 18, lines 61 – 66; where the control unit issues a command to read the data in a memory location in the DRAM and subsequently, the data is read from the DRAM into the local storage of the attached processing unit).

28. With respect to claim 22, the combination of Suzuoki and the admission teach of all the limitations of the parent claims as discussed supra. Suzuoki also teaches of means for transferring the data block from the secondary memory to the common

memory after processing the data block (fig. 24; items 2440, 2442; column 18, line 67 – column 19, line 4; where the APU issues a DMA command to store the result in the DRAM from the APU's local memory).

29. With respect to claim 23, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki also teaches of means for notifying one of the first processors after processing the data block (fig. 24; item 2444; column 19, line 4 – 6; where the APU issues an interrupt request to the PU to signal that the processing is complete).

30. With respect to claim 24, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki also teaches of means for requesting the secondary processor to process the data block (fig. 24; item 2410; column 18, lines 31 – 32; where the processing unit designates an APU to process the apulet).

31. With respect to claim 26, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki also teaches of means for processing the data block further (fig. 24; item 2410; column 18, lines 31 – 32; where the processing unit evaluates the apulet before designating an APU to process it).

32. Claims 7, 16, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuoki and the applicant's admitted prior art as applied to claims 1, 10, and 19 respectively, and further in view of Lee et al., U.S. Patent No. 6,128,724 (hereinafter Lee).

33. With respect to claim 7, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki teaches of wherein the dividing comprises dividing the common memory into data blocks (figs. 2, 24; item 2412; column 3, lines 43 – 53; column 7, lines 43 – 56; column 18, lines 32 – 35; where the processing unit allocates space in the DRAM for executing the apulet by issuing a DMA command to the DMAC to setup the necessary sandboxes. The sandboxes are exclusive areas in the DRAM that only a specific attached processing unit can access).

The combination of Suzuoki and the applicant's admission fail to specifically teach of a size of the data blocks equaling a size of registers of the available secondary processor. However, Lee teaches of a size of the data blocks equaling a size of registers of the available secondary processor (fig. 3b; column 5, lines 20 – 40; where a block transfer on a single register file in the computational unit, the data block can be a full register file).

The combination of Suzuoki and the applicant's admission, and Lee are analogous arts as they are both related to processing data and instruction in parallel. It would have been obvious to one of ordinary skill in the art having the teachings of Suzuoki, the applicant's admission, and Lee at the time of the invention to make the data blocks in the DRAM of Suzuoki the same size of the APU registers in Suzuoki just like the data blocks in Lee that are the same size as a full register file in the computation unit in Lee. The motivation for this would have been to reduce the complexity and reduce the amount of overhead on the hardware, Lee column 5, lines 32 – 40.

34. With respect to claim 16, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki teaches of wherein the one first processor is further adapted to divide the common memory into data blocks (figs. 2, 24; item 2412; column 3, lines 43 – 53; column 7, lines 43 – 56; column 18, lines 32 – 35; where the processing unit allocates space in the DRAM for executing the apulet by issuing a DMA command to the DMAC to setup the necessary sandboxes. The sandboxes are exclusive areas in the DRAM that only a specific attached processing unit can access).

The combination of Suzuoki and the applicant's admission fail to specifically teach of a size of the data blocks equaling a size of registers of the available secondary processor. However, Lee teaches of a size of the data blocks equaling a size of registers of one of the secondary processors (fig. 3b; column 5, lines 20 – 40; where a block transfer on a single register file in the computational unit, the data block can be a full register file).

35. With respect to claim 25, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki teaches of wherein the means for dividing comprises means for dividing the common memory into data blocks (figs. 2, 24; item 2412; column 3, lines 43 – 53; column 7, lines 43 – 56; column 18, lines 32 – 35; where the processing unit allocates space in the DRAM for executing the apulet by issuing a DMA command to the DMAC to setup the necessary sandboxes. The sandboxes are exclusive areas in the DRAM that only a specific attached processing unit can access).

The combination of Suzuoki and the applicant's admission fail to specifically teach of a size of the data blocks equaling a size of registers of the available secondary processor. However, Lee teaches of a size of the data blocks equaling a size of registers of the secondary processors (fig. 3b; column 5, lines 20 – 40; where a block transfer on a single register file in the computational unit, the data block can be a full register file).

36. Claims 9, 18, and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuoki and the applicant's admitted prior art as applied to claims 1, 10, and 19 respectively, and further in view of Proch et al., U.S. Patent No. 6,381,659 (hereinafter Proch).

37. With respect to claim 9, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki teaches of identifying, using one of the first processors, additional available secondary processors to process data blocks (figs. 24 – 26B; item 2410; column 7, lines 57 – 66; column 18, lines 31 – 32; column 19, line 38 – column 20, line 52; where the processing unit designates an attached processing unit to process the apulet. Also where the PU assigns 3 different APUs to process a network apulet and MPEG apulets).

The combination of Suzuoki and the applicant's admission fail to specifically teach of processing the data blocks until all the data blocks have been processed. However, Proch teaches of processing the data blocks until all the data blocks have been processed (column 5, lines 28 – 39; where the first data block is read. Then the

second data block is read. This is repeated until all the data blocks in the buffer have been read).

The combination of Suzuoki and the applicant's admission, and Proch are analogous arts as they are both involve processing data. It would have been obvious to one of ordinary skill in the art having the teachings of Suzuoki, the applicant's admission, and Proch at the time of the invention to incorporate the process/concept of processing data block until there are no more data blocks to process from Proch into the PU sorting out data blocks to the APUs in The combination of Suzuoki and the applicant's admission. The motivation for this would have been to allow for all of the data to be processed.

38. With respect to claim 18, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki teaches of wherein one the first processors is adapted to identify additional available secondary processors to process data blocks (figs. 24 – 26B; item 2410; column 7, lines 57 – 66; column 18, lines 31 – 32; column 19, line 38 – column 20, line 52; where the processing unit designates an attached processing unit to process the apulet. Also where the PU assigns 3 different APUs to process a network apulet and MPEG apulets).

The combination of Suzuoki and the applicant's admission fail to specifically teach of processing the data blocks until all the data blocks have been processed. However, Proch teaches of processing the data blocks until all the data blocks have been processed (column 5, lines 28 – 39; where the first data block is read. Then the

second data block is read. This is repeated until all the data blocks in the buffer have been read).

39. With respect to claim 27, the combination of Suzuoki and the admission teach of all the limitations of the parent claim as discussed supra. Suzuoki teaches of means for identifying additional available secondary processors to process data blocks (figs. 24 – 26B; item 2410; column 7, lines 57 – 66; column 18, lines 31 – 32; column 19, line 38 – column 20, line 52; where the processing unit designates an attached processing unit to process the apulet. Also where the PU assigns 3 different APUs to process a network apulet and MPEG apulets).

The combination of Suzuoki and the applicant's admission fail to specifically teach of processing the data blocks until all the data blocks have been processed. However, Proch teaches of processing the data blocks until all the data blocks have been processed (column 5, lines 28 – 39; where the first data block is read. Then the second data block is read. This is repeated until all the data blocks in the buffer have been read).

Double Patenting

40. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double

patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

41. Claims 1 – 5, 7 – 8, 10 – 17, 19, and 25 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 4 – 9, 12 – 17, and 20 of copending Application No. 10/670,837. Although the conflicting claims are not identical, they are not patentably distinct from each other. See chart below.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Application 10/670,840	**Application 10/670,837**
Claim 1: A computer-implemented method for handling data using a plurality of processors, the method comprising: dividing a common memory, accessible to one or more first processors and to one or more secondary processors, into a plurality of data blocks using one of the first processors,	Claim 1: A computer-implemented method for solving linear equations, the method comprising: receiving, into a common memory, a plurality of coefficients, the common memory being accessible by one or more first processors and by one or more secondary processors, dividing the coefficients into a plurality of coefficient blocks using the one or more first processors;
the one or more first processors and the one or more second processors being chosen from a group of heterogeneous processors;	the one or more first processors and the one or more second processors being chosen from a group of heterogeneous processors

identifying an available processor from the secondary processors to process one of the data blocks;	identifying an available processor from the secondary processors for processing one of the coefficient blocks;
and processing the data block using the available secondary processor.	processing the coefficient block using the available secondary processor
Claim 2	Claim 4
Claim 3	Claim 4
Claim 4	Claim 1
Claim 5	Claim 7
Claim 7	Claim 5
Claim 8	Claim 8
Claim 10: An information handling system comprising: a plurality of heterogeneous processors,	Claim 9: An information handling system comprising: a plurality of heterogeneous processors,
wherein the plurality of heterogeneous processors comprises one or more first processors and one or more secondary processors;	wherein the plurality of heterogeneous processors includes one or more first processors and one or more secondary processors;
and a common memory accessible by the plurality of heterogeneous processors	and a common memory accessible by the plurality of heterogeneous processors
one of the first processors is adapted to divide the common memory into a plurality of data blocks	one of the first processors is adapted to receive, into the common memory, a plurality of coefficients, the coefficients corresponding to the linear equations, one of the first processors is adapted to divide the coefficients into a plurality of coefficient blocks
one of the first processors is adapted to identify an available processor from the secondary processors to process one of the data block;	one of the first processors is adapted to identify an available processor from the secondary processors for processing one of the coefficient blocks
and one of the secondary processors is adapted to process the data block.	the available secondary processor is adapted to process the coefficient block
Claim 11	Claim 12
Claim 12	Claim 12

Claim 13	Claim 9
Claim 14	Claim 15
Claim 15	Claim 14
Claim 16	Claim 13
Claim 17	Claim 16
Claim 19: A computer program product on computer operable media, the computer program product comprising: means for dividing a common memory, accessible to one or more first processors and to one or more secondary processors, into a plurality of data blocks,	Claim 17: A computer program product on computer operable media, the computer program product comprising: means for receiving, into a common memory, a plurality of coefficients, the common memory being accessible by one or more first processors and by one or more secondary processors, means for dividing the coefficients into a plurality of coefficient blocks;
wherein the one or more first processors and the one or more second processors are selected from a group of heterogeneous processors;	wherein the one or more first processors and the one or more second processors are included in a group of heterogeneous processors
means for identifying an available processor from the secondary processors to process one of the data blocks;	means for identifying an available processor from the secondary processors for processing one of the coefficient blocks;
means for processing the data block using the available secondary processor.	means for processing the coefficient block,
Claim 25	Claim 20

Conclusion

42. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

43. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

44. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

45. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Krofcheck

MATTHEW D. ANDERSON
PRIMARY EXAMINER